AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Currently Amended) A method of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system comprising:

transmitting a first digital signal along the first signal path;

transmitting a second digital signal along the second signal path wherein the second digital signal has a value opposite a value of the first digital signal;

storing the second signal in a buffer along the second signal path;

inverting the value of the first digital signal along the first signal path to match the value of second digital signal; and

re-inverting the first digital signal along the first signal path at a final destination of the first signal path.

2. (Currently Amended) The method of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 1 further comprising:

~~storing the second signal in a buffer along the second signal path~~ time delaying at least one of the first and second digital signals with a time delay circuit.

3. (Currently Amended) The method of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim [[2]] 1 wherein inverting the first digital signal takes place when storing the second signal.

4. (Original) The method of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 1 further comprising:

repeating the first digital signal along the first path; and

repeating the second digital signal along the second path.

5. (Currently Amended) The method of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim [[2]] 1 further comprising:

a first signal repeater that repeats the first digital signal after the first digital signal is inverted; and

a second signal repeater that repeats the second digital signal after the second digital signal is stored.

6. (Original) The method of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 1 wherein

the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

7. (Original) The method of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 2 wherein

the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

8. (Original) The method of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 3 wherein

the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

9. (Original) The method of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 4 wherein

the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

10. (Original) The method of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 5 wherein

the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

11. (Original) The method of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 6 wherein

the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

12. (Currently Amended) An electrical transmission circuit comprised of:

a sending device transmitting a first digital signal having a value along a first signal path;

a second device transmitting a second digital signal having a value opposite the value of the first digital signal along a second signal path;

a buffer device along the second signal path that stores the value of the second digital signal;

an inverter device that inverts the value of the first digital signal to match the value of the second digital signal; and

a receiving device that receives the first digital signal and the second digital signal wherein the receiving device inverts the value of the first digital signal.

13. (Currently Amended) The electrical transmission circuit of claim 12 further comprised of:

~~a buffer device along the second signal path that stores the value of the second digital signal~~ at least one time delay circuit incorporated in at least one of the first and second signal paths for delaying at least one of the first and second digital signals.

14. (Currently Amended) The electrical transmission circuit of claim [[13]] 12 wherein the inverter is placed opposite the buffer device.

15. (Original) The electrical transmission circuit of claim 12 further comprised of:

a first repeater device that repeats the first digital signal along the first signal path; and

a second repeater device that repeats the second digital signal along the second signal path.

16. (Currently Amended) The electrical transmission circuit of claim [[13]] 12 further comprised of:

a first repeater device that repeats the first digital signal after the first digital signal is inverted; and

a second repeater devices that repeats the second digital signal after the second digital signal is stored.

17. (Original) The electrical transmission circuit of claim 12 wherein the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

18. (Original) The electrical transmission circuit of claim 13 wherein the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

19. (Original) The electrical transmission circuit of claim 14 wherein the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

20. (Original) The electrical transmission circuit of claim 15 wherein the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

21. (Original) The electrical transmission circuit of claim 16 wherein the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

22. (Currently Amended) An apparatus of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system comprised of:

means for transmitting a first digital signal along the first signal path;

means for transmitting a second digital signal along the second signal path wherein the second digital signal has a value opposite a value of the first digital signal;

means for storing the second digital signal in a buffer along the second signal path;

means for inverting the value of the first digital signal along the first signal path to match the value of second digital signal; and

means for re-inverting the first digital signal along the first signal path at a final destination of the first signal path.

23. (Currently Amended) The apparatus of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 22 further comprised of:

~~means for storing the second digital signal in a buffer along the second signal path~~ means for time delaying at least one of the first and second digital signals.

24. (Currently Amended) The apparatus of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim [[23]] 22 wherein the means for inverting the first digital signal takes place when storing the second digital signal.

25. (Original) The apparatus of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 22 further comprised of:

means for repeating the first digital signal; and

means for repeating the second digital signal.

26. (Currently Amended) The apparatus of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim [[23]] 22 further comprised of:

means for repeating the first digital signal after inverting the first digital signal; and

means for repeating the second digital signal after storing the second digital signal.

27. (Original) The apparatus of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 22 wherein the value of

the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

28. (Original) The apparatus of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 23 wherein the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

29. (Original) The apparatus of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 24 wherein the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

30. (Original) The apparatus of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 25 wherein the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.

31. (Original) The apparatus of minimizing coupling capacitance interference between a first signal path and a second signal path in an electrical system of claim 26 wherein the value of the first digital signal and the value of the second digital signal are the same for at least one half of the first signal path.